ABSTRACT

An integrated circuit device having a plurality of input terminals comprises: a plurality of input buffers provided in correspondence to the plurality of input terminals; a plurality of serial parallel conversion circuits for converting, in serial-parallel, outputs of the input buffers, respectively; and a plurality of boundary scan registers which are provided in correspondence to each input terminal. The output of the input buffer is supplied to the serial parallel conversion circuit and the boundary scan register in parallel, to restrict a delay element between the input buffer and the serial parallel conversion circuit at a minimum.